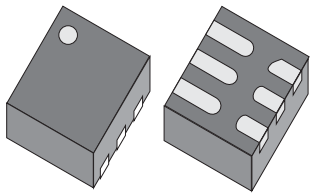
ECMF02-2HSMX6

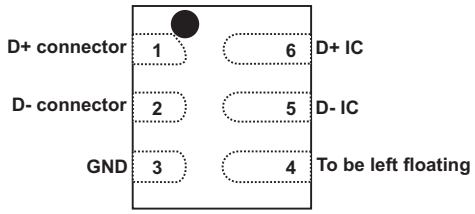
ESD protected common mode filter for USB3.0 interface

Datasheet - production data



µQFN-6L 1.7 x 1.5 mm

Figure 1. Pin out, top view



Features

- High common mode attenuation:
  - -10 dB @ 300 MHz
  - -20 dB @ 2.4 and 5 GHz
  - -15 dB from 500 MHz to 6 GHz
- Compliant with USB3.0 eye diagram
- Small and thin package 1.5 x 1.7 x 0.5 mm
- RoHS compliant.
- High reduction of parasitic elements through integration.
- ESD protection compliant with IEC 61000-4-2 level 4 standards (8 kV contact)

Benefits

- Suppress the common mode noise but keep signal integrity
- Low PCB space consumption.
- Save components count
- Make the application robust against ESD strikes from external environment

Description

The ECMF02-2HSMX6 is a highly integrated common mode filter designed to suppress EMI/RFI common mode noise on high speed differential serial buses like the USB3.0 transceiver.

Applications

Consumer and computer electronics featuring USB3.0 such as:

- Personal computer
- Notebook
- Tablet
- Set-top boxes
- PC graphic cards
- Telecom application

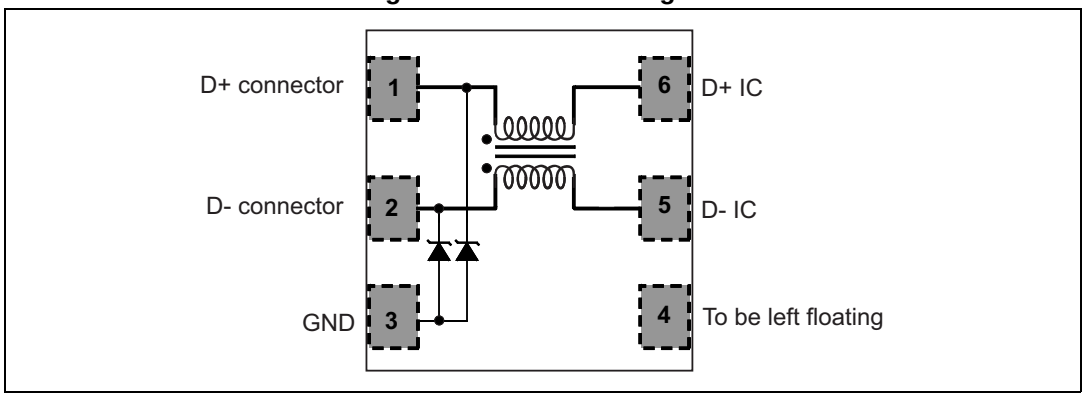
1 Functional description

The ECMF02-2HSMX6 is an ESD protected common mode filter especially designed for USB3.0 Tx/Rx differential pair, for host and device. The USB3.0 is actually made of 3 differential pairs. The first differential pair supports the high speed USB mode (also called USB2.0 mode). The 2 other differential pairs are used to support the super speed USB mode in full duplex. Bit rate on super speed USB can reach 5 Gbps. The ECMF02-2HSMX6 is able to filter the common mode noise from 300 MHz to 6 GHz, helping to make the application compliant with the electromagnetic interference emission standard such as CISPR22 or FCC part 15, or EN55022 and avoiding antenna desense on mobile phones, WiFi/Bluetooth, GPS,/GNSS frequencies. At the same time, the ECMF02-2HSMX6 keeps the high speed signal integrity and provides an efficient ESD protection.

More application information available in following AN:

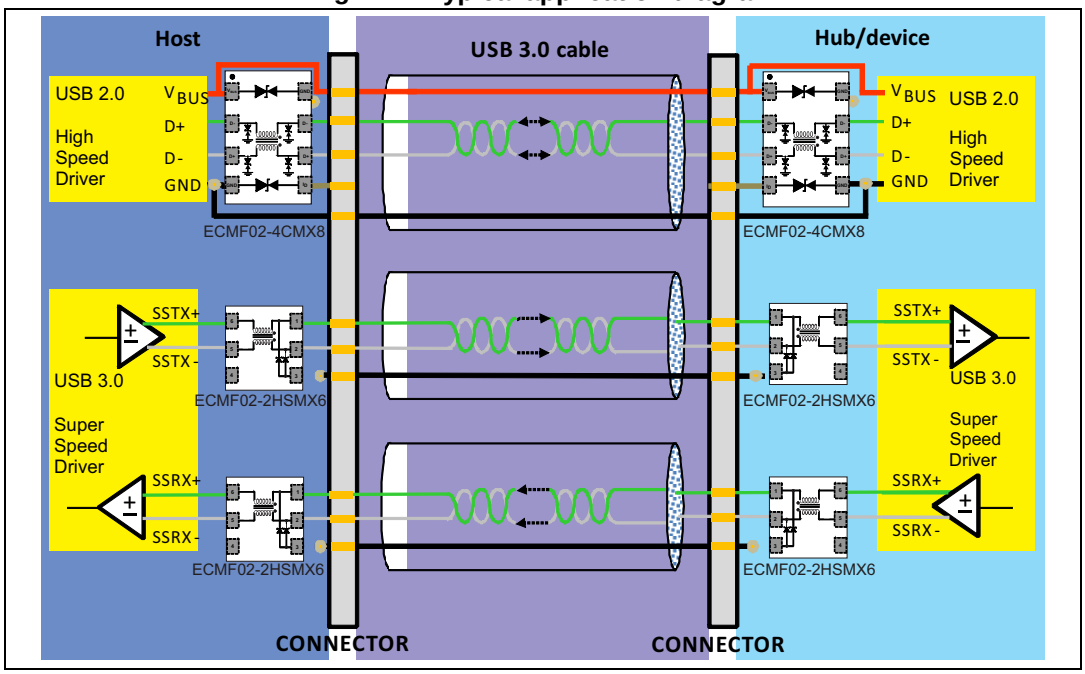
- Application Note AN4356: "Antenna desense on handheld equipment"
- Application Note AN4511: "Common Mode filters"
- Application Note AN4540: "MHL link filtering and protection"

Figure 2. Functional diagram



A typical application diagram is shown in *Figure 3*. ST offers a global approach to USB3.0 interface by providing a comprehensive range of dedicated products.

Figure 3. Typical application diagram



2 Electrical characteristics

Table 1. Absolute maximum ratings (limiting values)

Symbol	Parameter	Test conditions	Value.	Unit
V_{PP}	ESD discharge (pins 1 and 2) IEC 61000-4-2 level 4	Contact discharge	±8	kV
		Air discharge	±15	kV
I_{DC}	Maximum DC current		100	mA
T_{OP}	Operating temperature range		-40 to 85	°C
T_J	Maximum junction temperature		125	°C
T_{stg}	Storage temperature range		-55 to +150	°C

Figure 4. Electrical characteristics (definitions)

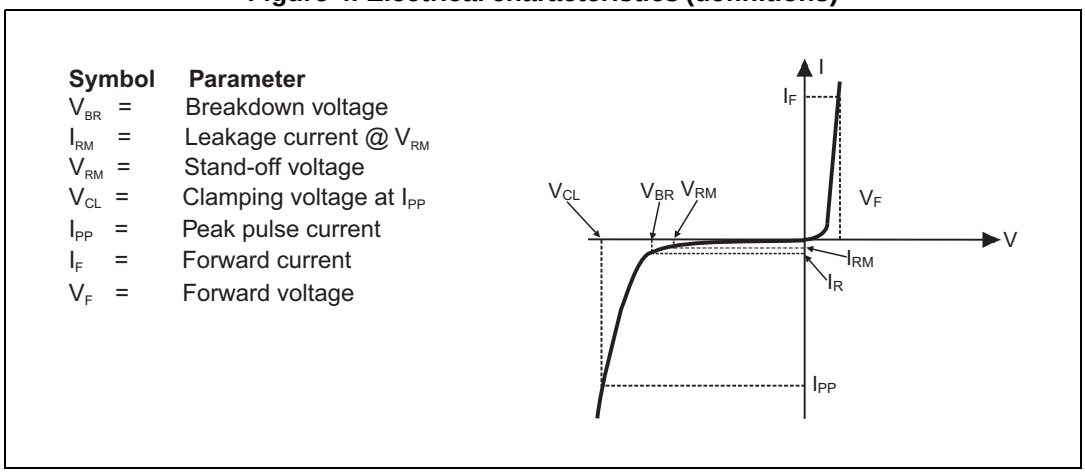


Table 2. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	Breakdown voltage	I_R = 1 mA	6			V
I_{RM}	Reverse leakage	V_{RM} = 3 V			100	nA
R_{DC}	DC serial resistance			7	9	Ω

Figure 5 shows that USB3.0 devices and cables can interfere with radio frequency devices operating between 700 MHz and 5 GHz.

Figure 5. USB3.0 frequency radiation measured with current loop

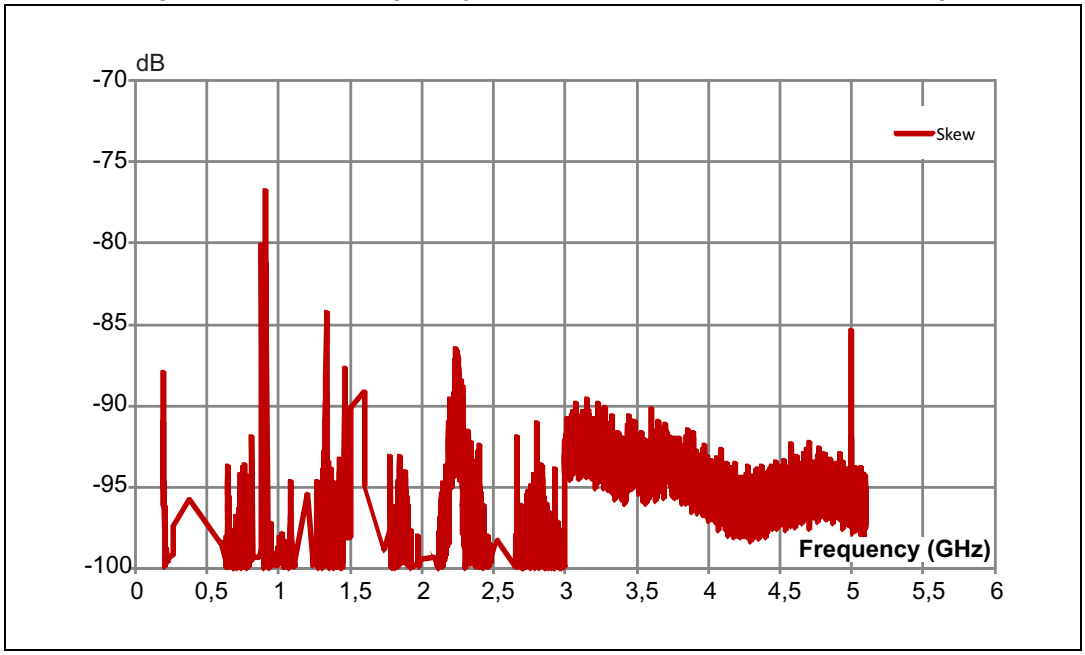


Figure 6. Differential attenuation versus frequency

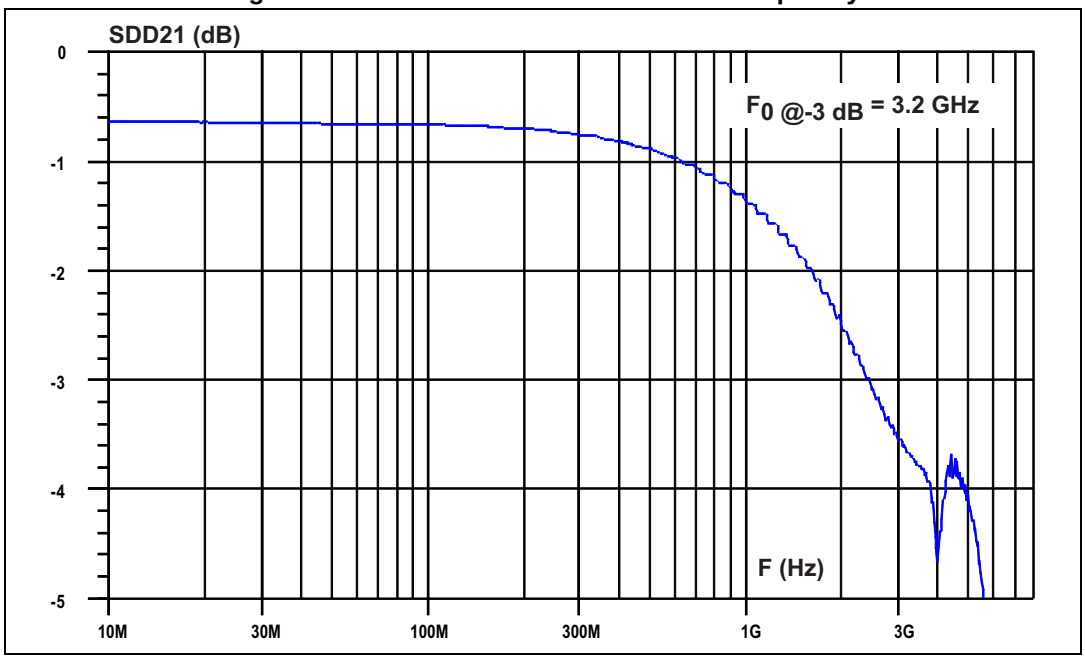
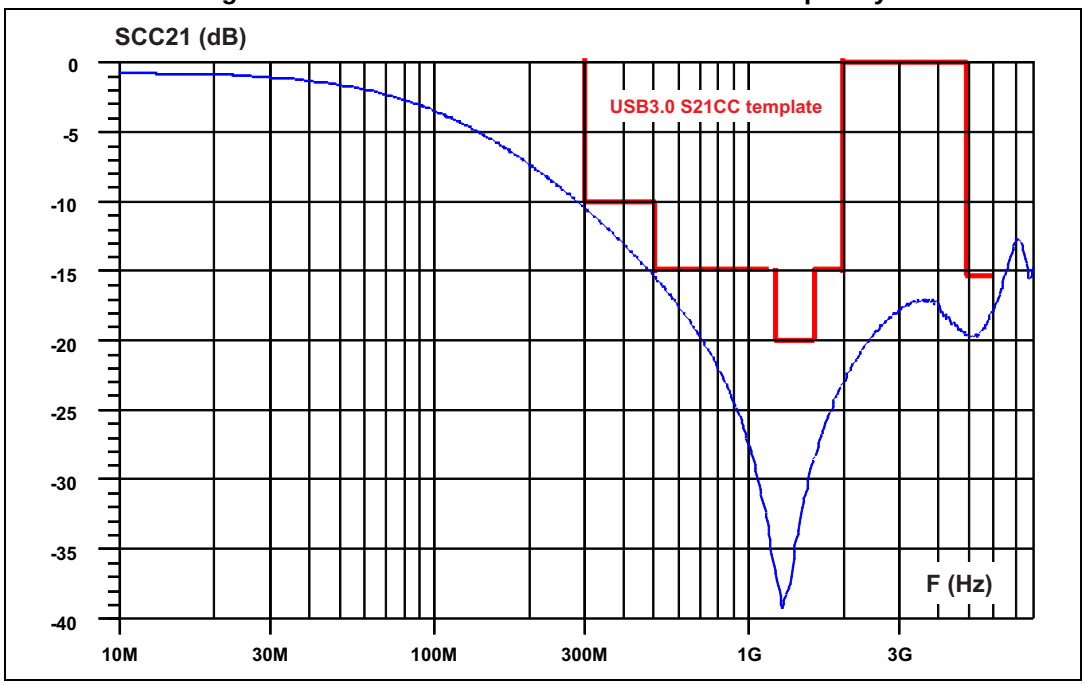


Figure 7. Common mode attenuation versus frequency



Note: STMicroelectronics has defined the USB3.0 SCC21 template to prevent antenna desense between 700 MHz and 5 GHz.

Figure 8. Return loss versus frequency ($Z_{0\ COM}$ = 50 Ω - SDD11)

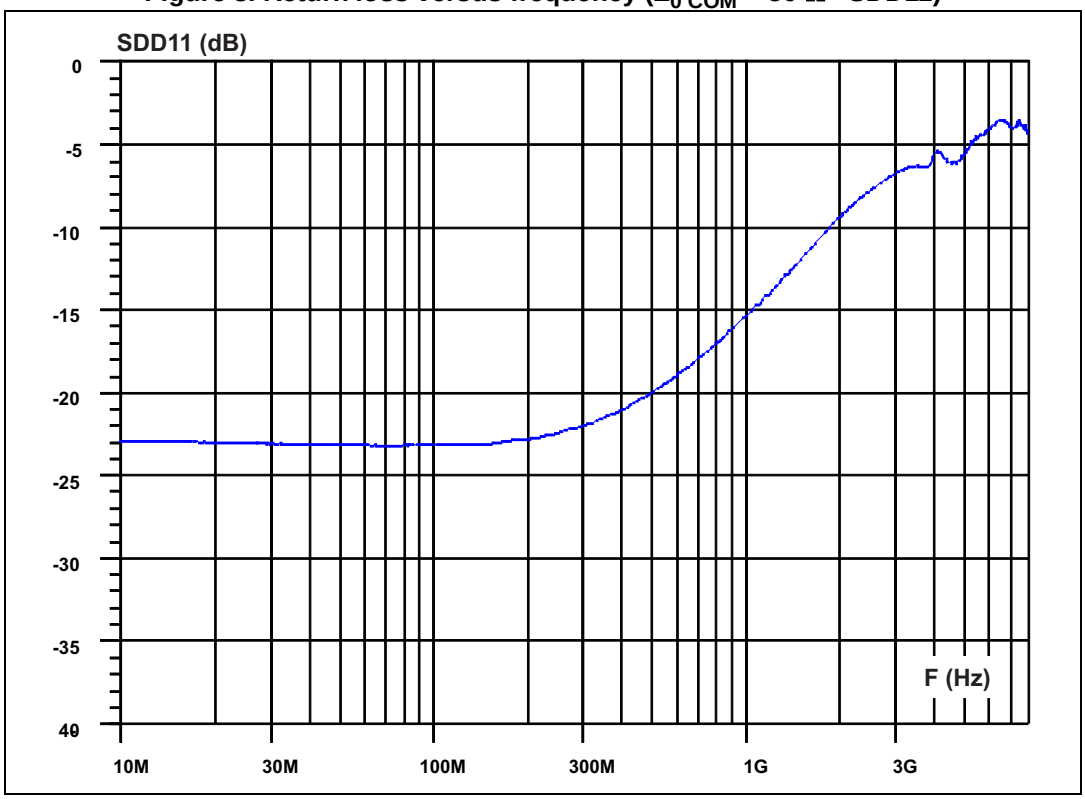


Figure 9. Return loss versus frequency ($Z_{0\ COM}$ = 50 Ω - SDD22)

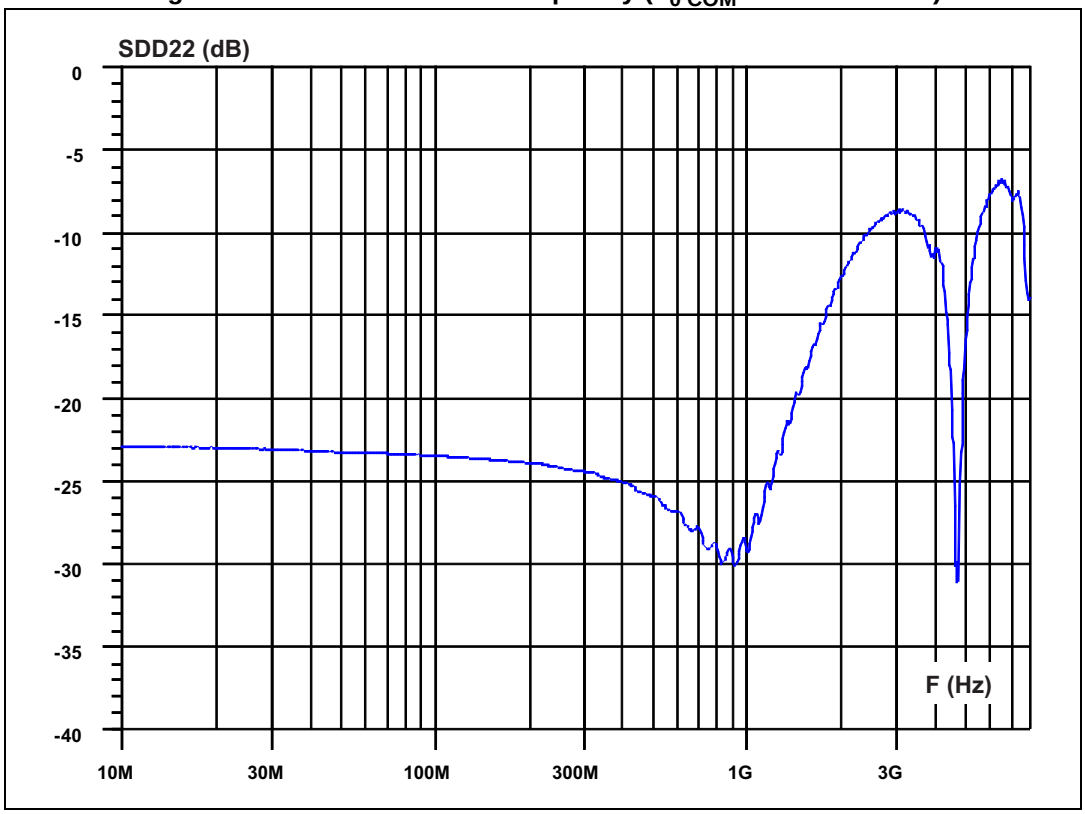


Figure 10. Differential (Z_{DD21}) and common mode (Z_{CC21}) impedance versus frequency

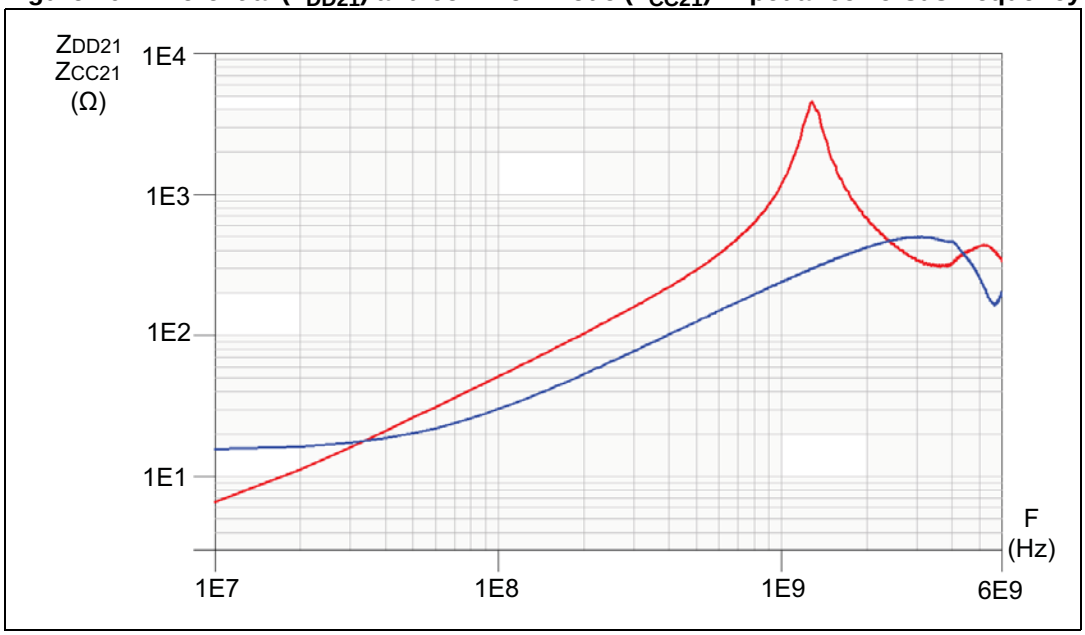


Figure 11. Typical ESD response to IEC 61000-4-2 +8kV contact

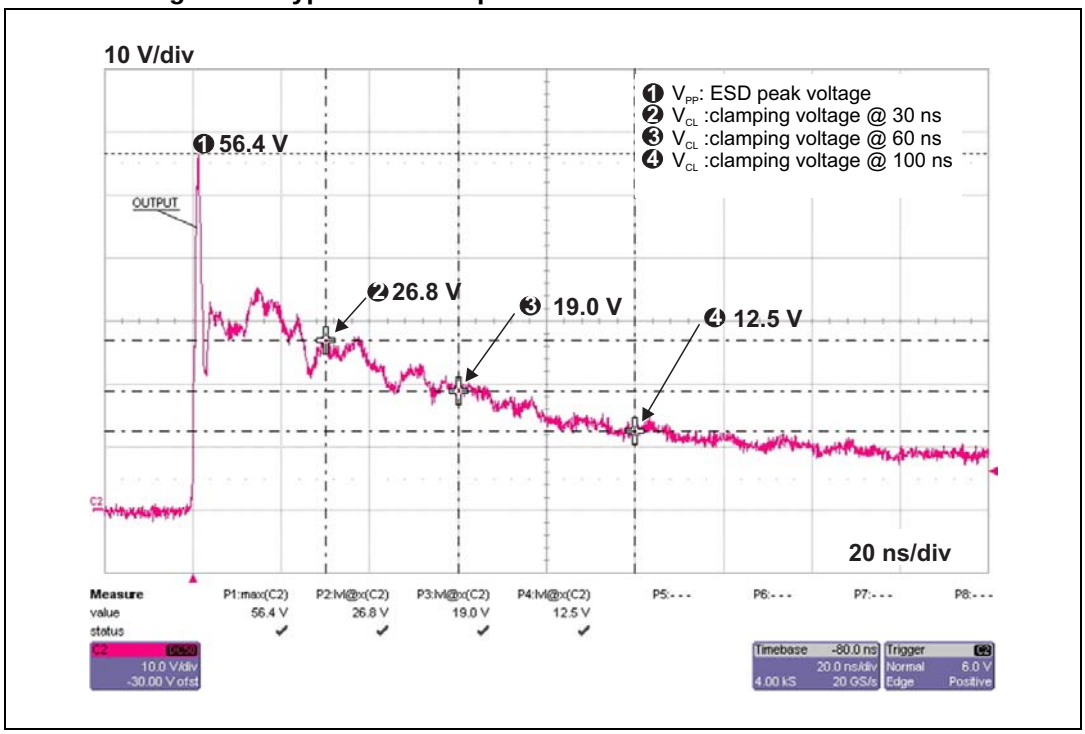


Figure 12. Typical ESD response to IEC 61000-4-2 -8kV contact

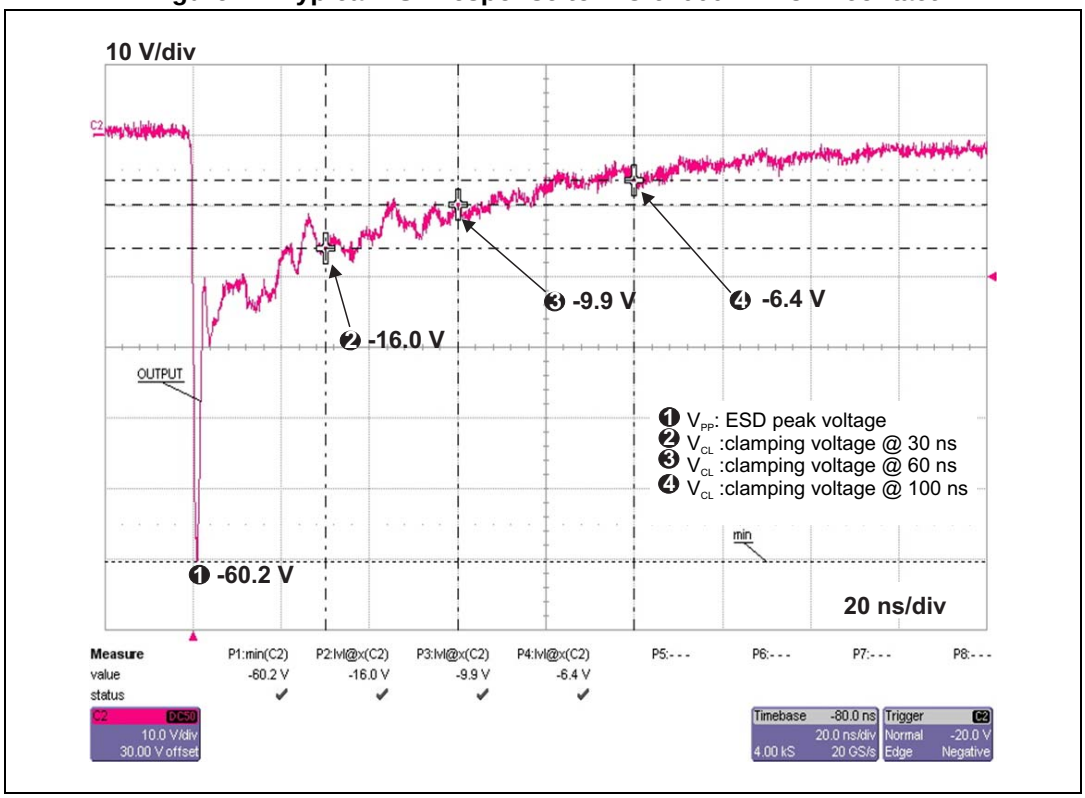


Figure 13. USB2.0 (480 Mbps) eye diagram without device

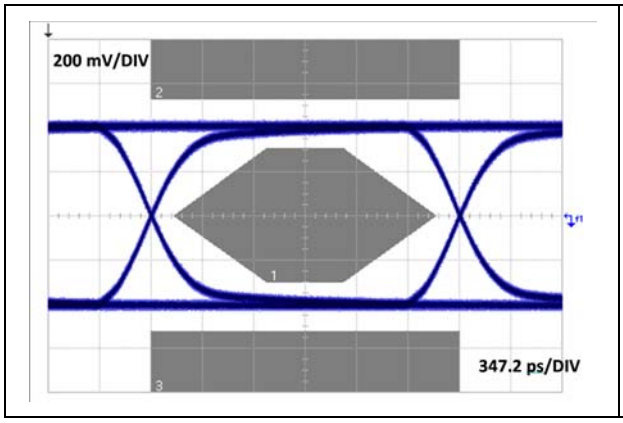


Figure 14. USB2.0 (480 Mbps) eye diagram with device

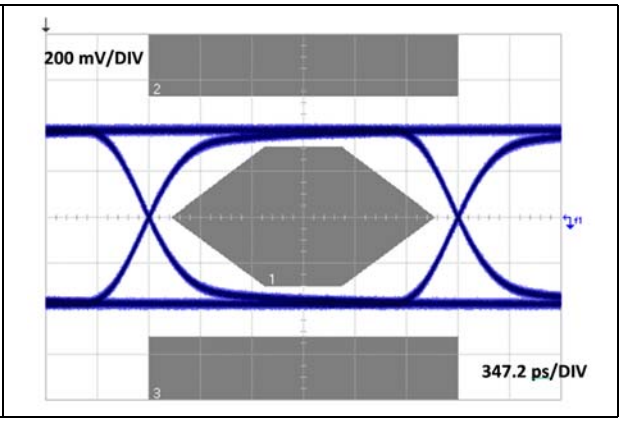


Figure 15. USB3.0 (5 Gbps) eye diagram without device

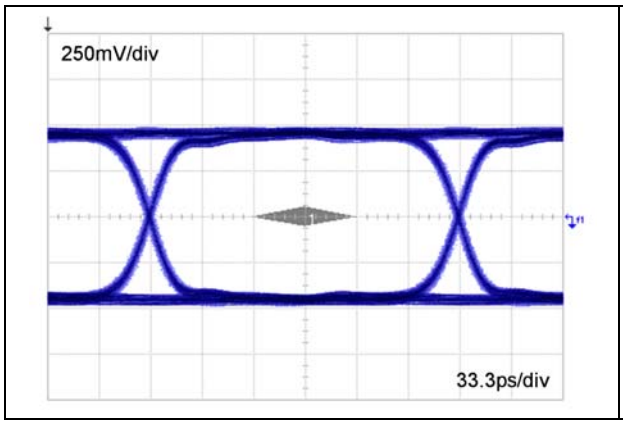


Figure 16. USB3.0 (5 Gbps) eye diagram with device

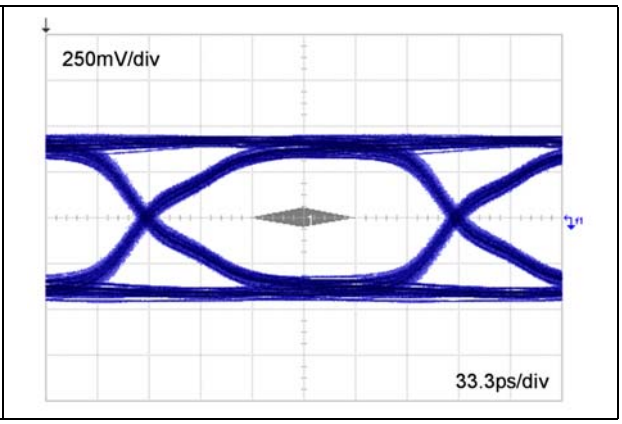


Figure 17. USB3.1 (10 Gbps) eye diagram without device

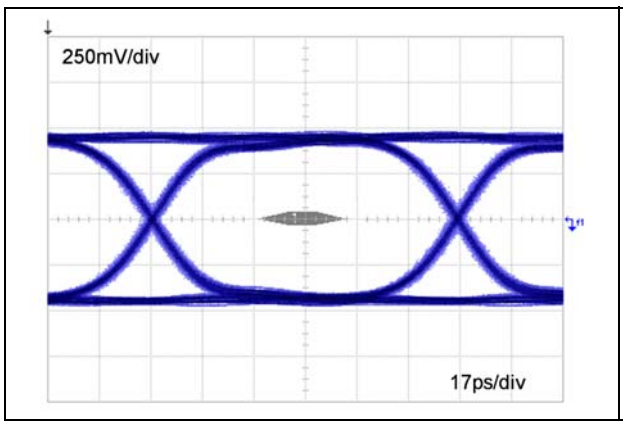


Figure 18. USB3.1 (10 Gbps) eye diagram with device

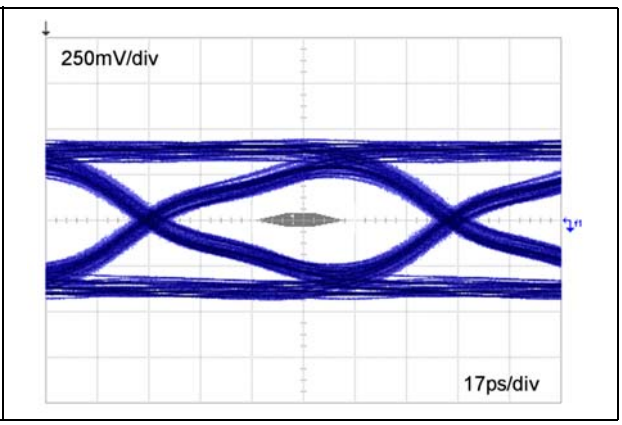


Figure 19. MHL (4.5 Gbps) eye diagram without device

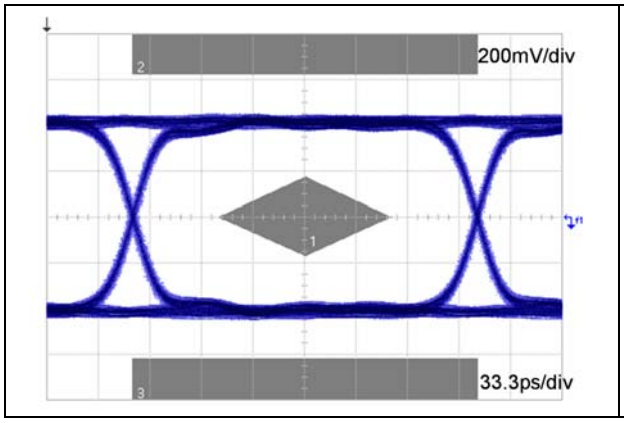


Figure 20. MHL (4.5 Gbps) eye diagram with device

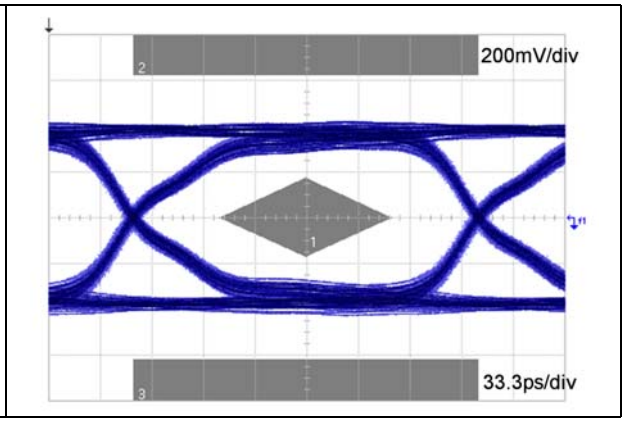


Figure 21. MHL (6 Gbps) eye diagram without device

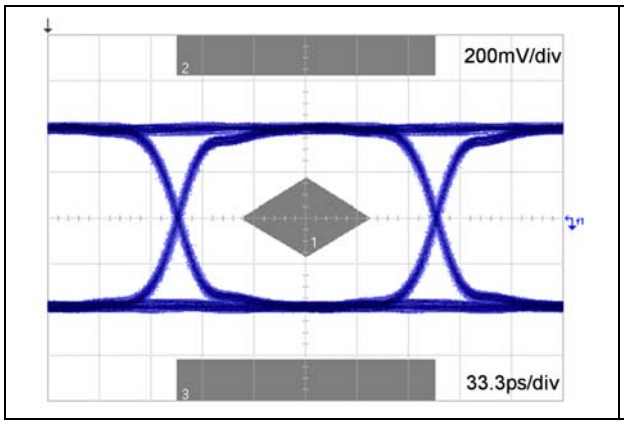


Figure 22. MHL (6 Gbps) eye diagram with device

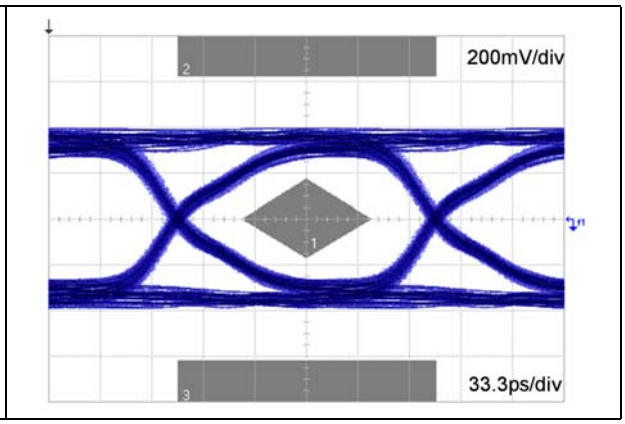


Figure 23. Display Port HBR2 (5.4 Gbps) eye diagram without device

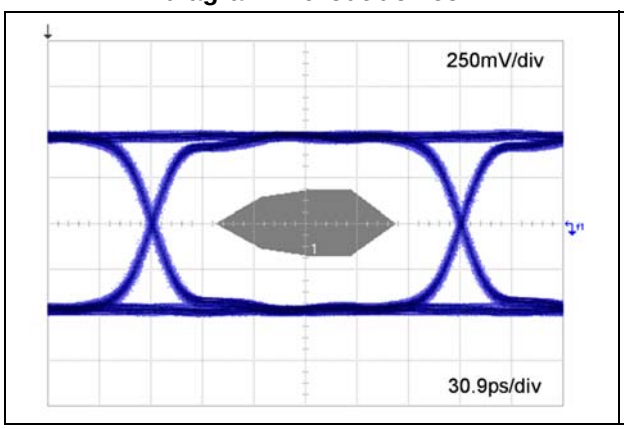
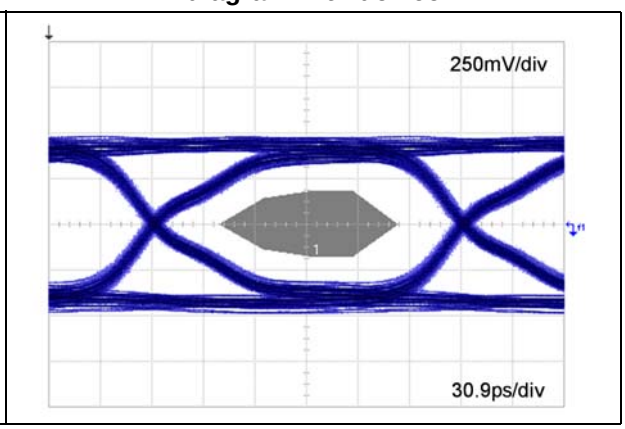


Figure 24. Display Port HBR2 (5.4 Gbps) eye diagram with device



3 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 25. µQFN-6L dimension definitions

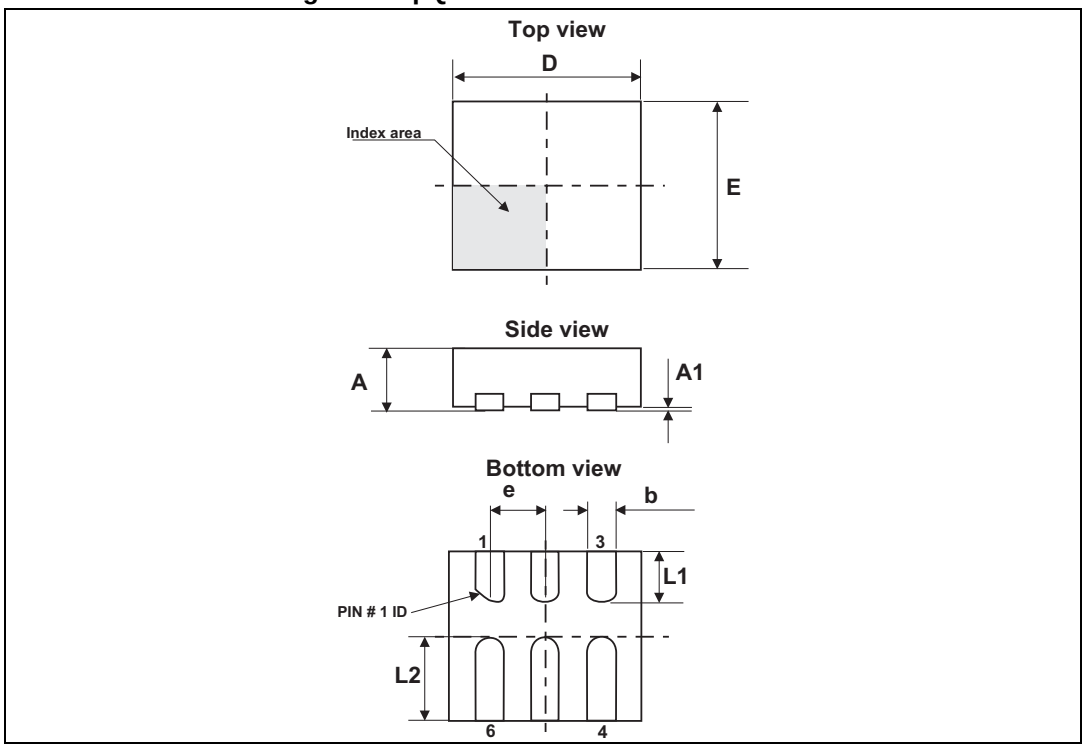


Table 3. µQFN-6L dimension values

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.45	0.50	0.55	0.018	0.020	0.022
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
D	1.55	1.60	1.65	0.061	0.063	0.065
E	1.30	1.35	1.40	0.051	0.053	0.055
e	0.45	0.50	0.55	0.018	0.020	0.022
L1	0.35	0.45	0.55	0.014	0.018	0.022
L2	0.65	0.75	0.85	0.026	0.030	0.034

Figure 26. Footprint, dimensions in mm (inches)

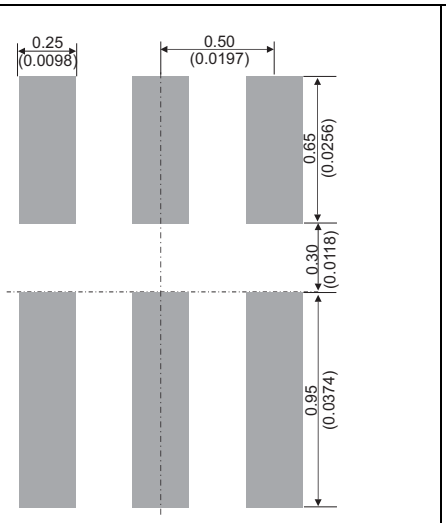


Figure 27. Marking

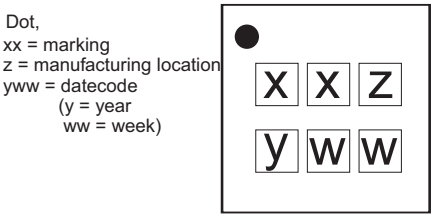
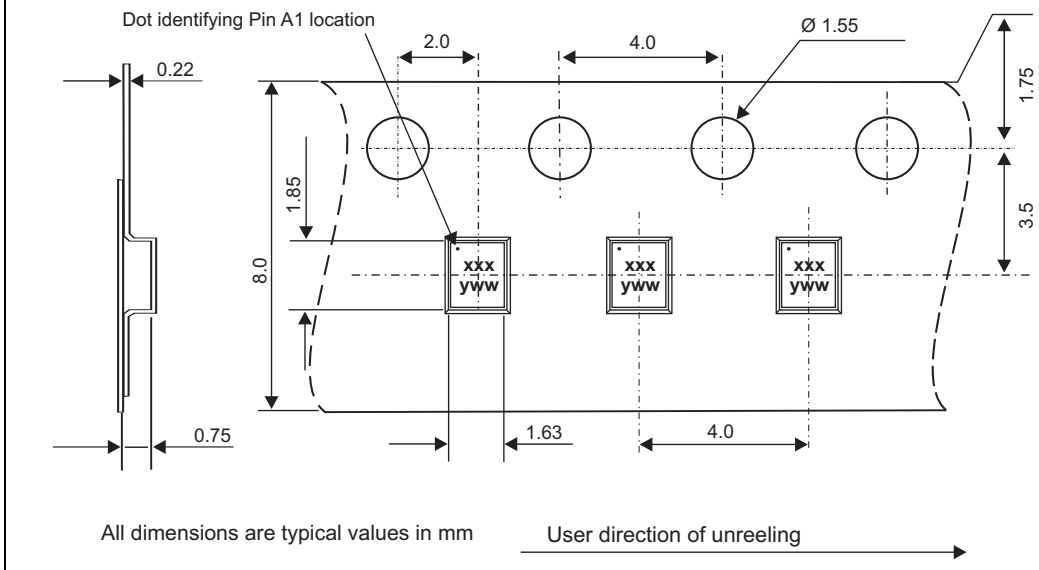


Figure 28. Tape and reel specifications

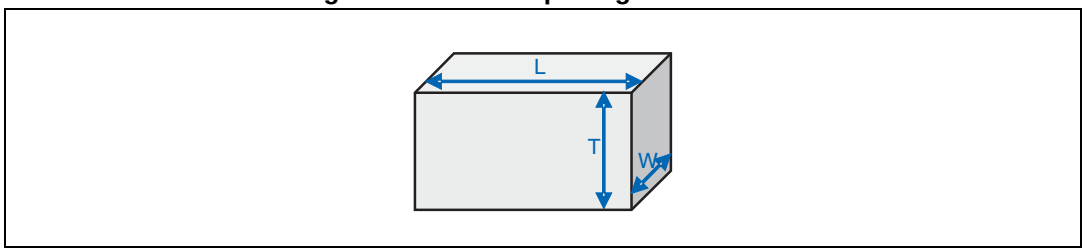


4 Recommendation on PCB assembly

4.1 Stencil opening design

1. General recommendation on stencil opening design
   a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

Figure 29. Stencil opening dimensions



   b) General design rule
   Stencil thickness (T) = 75 ~ 125 µm

$$\text{Aspect Ratio} = \frac{W}{T} \geq 1.5$$

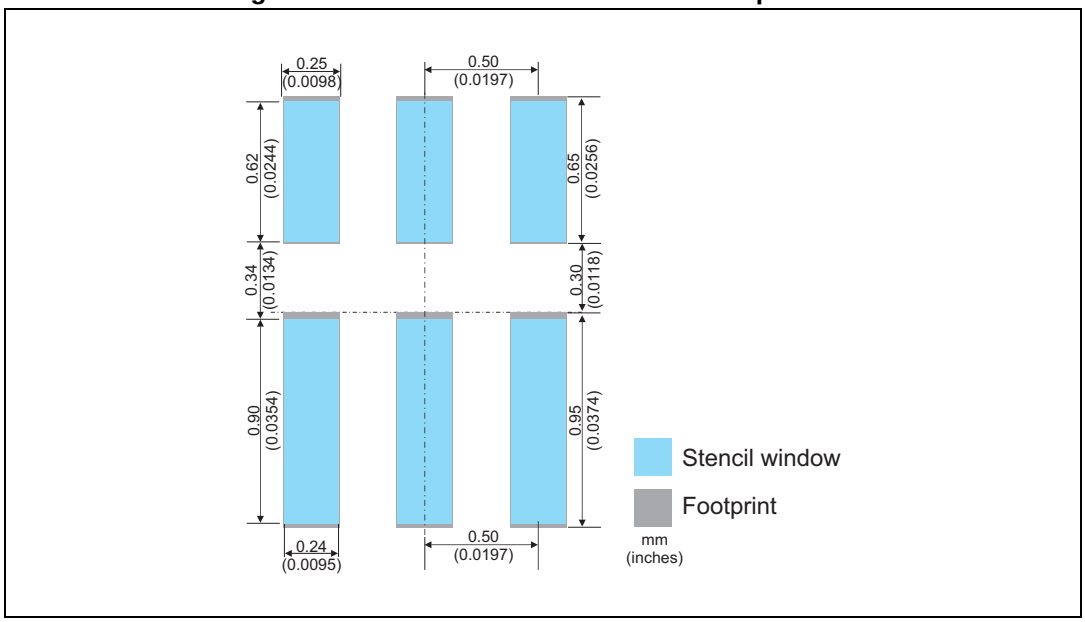
$$\text{Aspect Area} = \frac{L \times W}{2T(L + W)} \geq 0.66$$

2. Reference design
   a) Stencil opening thickness: 100 µm
   b) Stencil opening for leads: Opening to footprint ratio is 90%.

4.2 Solder paste

1. Use halide-free flux, qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste recommended.
3. Offers a high tack force to resist component displacement during PCB movement.
4. Use solder paste with fine particles: powder particle size 20-45 µm.

Figure 30. Recommended stencil window position



4.3 Placement

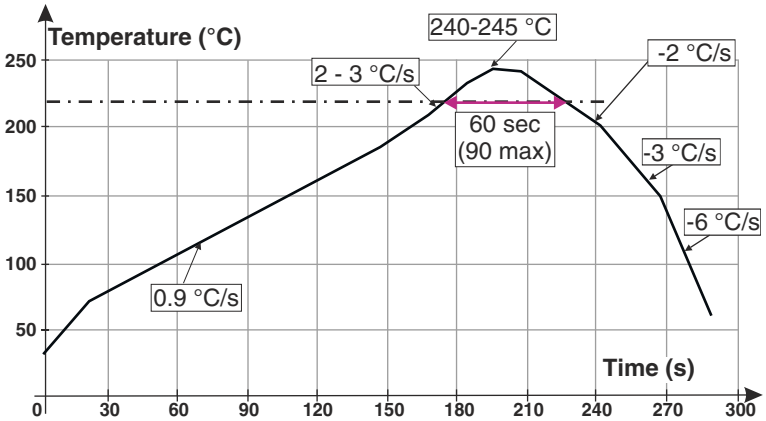
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

4.5 Reflow profile

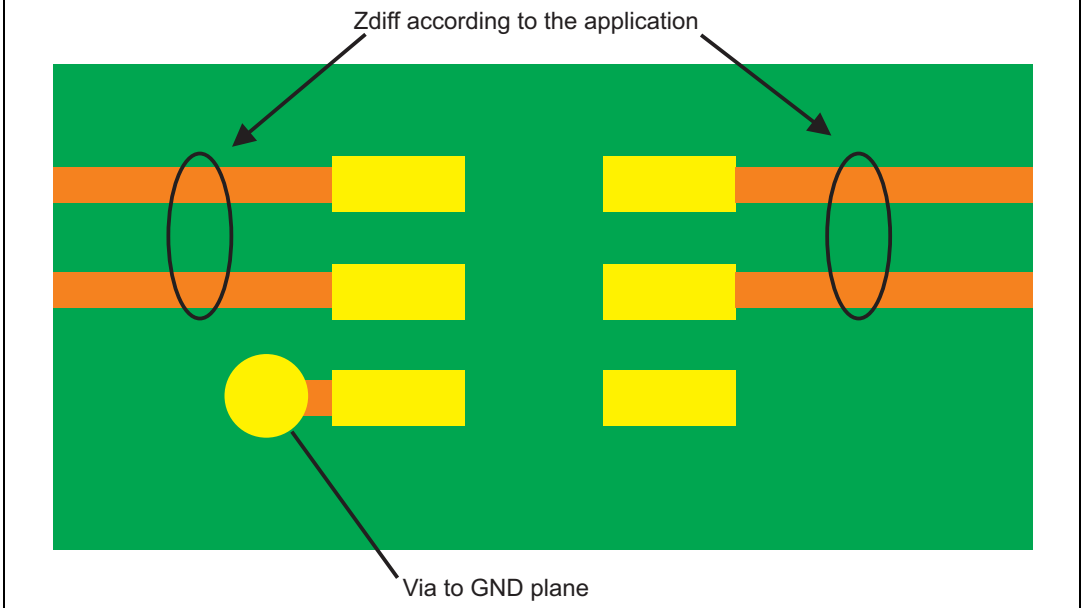
Figure 31. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

4.6 PCB layout recommendation

Figure 32. PCB footprint recommendation



5 Ordering information

Figure 33. Ordering information scheme

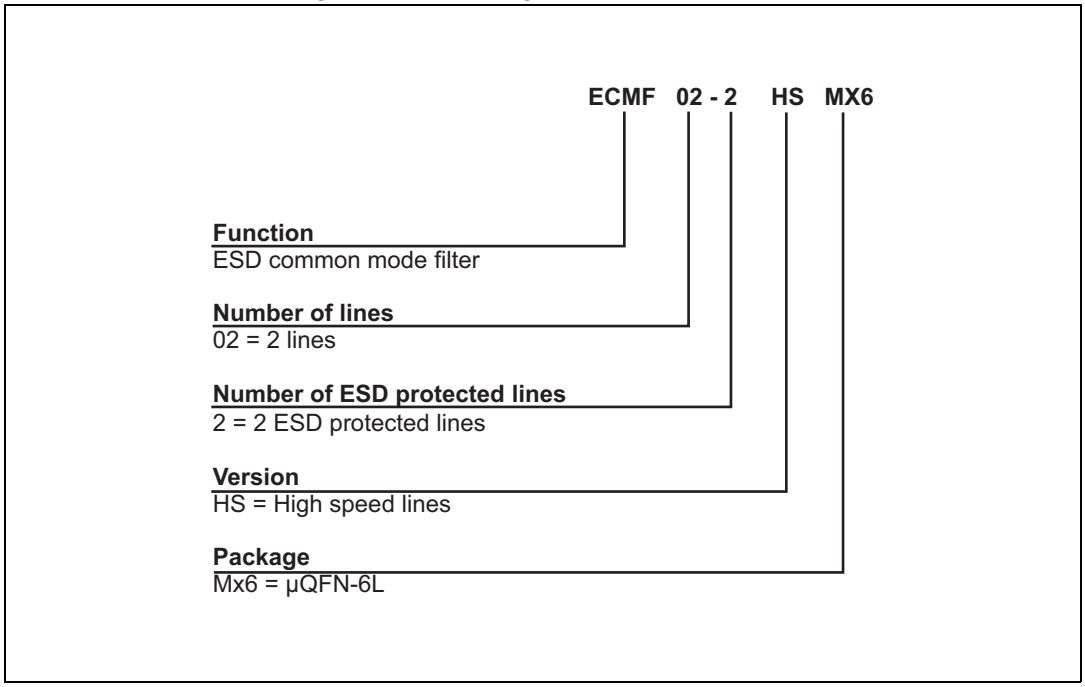


Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
ECMF02-2HSMX6	KR	µQFN-6L	3.4 mg	3000	Tape and reel

6 Revision history

Table 5. Document revision history

Date	Revision	Changes
13-Nov-2013	1	Initial release.
25-Aug-2014	2	Inserted *Figure 10: Differential (ZDD21) and common mode (ZCC21) impedance versus frequency*.